REMARKS

In response to the Office Action dated March 29, 2010, Applicant requests consideration of the following remarks. Applicant has amended claims 1, 9, 10, 13, 17, 18, and 22. No new matter is introduced as a result of the amendments. Claims 18-21 are hereby cancelled, and claims 5, 8, and 16 were previously cancelled. Claims 1-4, 6, 7, 9-15, 17, and 22 are currently pending in the application.

I. Claim Rejections - 35 U.S.C. § 103

Rejection of Claims 1-4, 6-7, 9-15, 17, and 22:

Claims 1-4, 6-7, 9-15, 17, and 22 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent Publication No. 2002/0176489 to Sririam et al. (herein "Sririam") in view of U.S. Patent No. 6,108,693 to Tamura (herein "Tamura") and U.S. Patent No. 6,928,575 to Okabayashi et al. (herein "Okabayashi"). Applicant has amended claims 1, 9, 10, 13, 17, and 22, from which the remaining rejected claims depend, and respectfully traverses this rejection.

Sririam discloses a vector correlator based Rake receiver that employs a circular buffer (para. [0007]). Two of the three buffers are available for processing by a correlator datapath while the remaining buffer is being written into by incoming chips (para. 0009]). The triple data buffer implements a sliding buffer of 16-chips in which the buffer slides by an interval of 16-chips in a circular fashion in each iteration (FIG. 1 and para. 0040]). At each correlator co-processor (CCP) iteration, 32-chips from the 48-chip triple data input buffer 100 are available for processing by the CCP datapath. At the next iteration, a new set of 16-chips, along with an older set of 16-chips, becomes available to the datapath (FIG. 1 and para. [0040]).

Tamura discloses a system and method of data communication between processors in a multiprocessor system that includes a transmitting processor, a receiving processor, and a shared memory (col. 2, lines 14-18). Two communication buffers are defined in the shared memory, and the transmitting buffer includes communication buffer selecting means for selecting one of the two communication buffers, and write inhibit means for changing the selected communication buffer to a write-disabled state in order to inhibit writing of the selected communication buffer by other processors (col. 2, lines 19-25). The receiving

processor includes communication buffer selecting means for selecting one of the two communication buffers, and read wait means for causing the receiving processor to wait until the selected communication buffer attains a read-enabled state (col. 2, lines 33-40). During the time that the transmitting processor is writing part of a message to a communication buffer, the receiving processor, even though it is capable of reception, cannot read in the message until writing is finished (col. 1, lines 50-58). However, the communication buffer selecting means of the transmitting buffer writes data by alternately selecting first and second communication buffers, and the buffer selecting means of the receiving processor reads in data by alternately selecting the first and second communication buffers (col. 2, lines 46-55).

Okabayashi discloses an LSI chip 100 on which a first processor 110, a second processor 120, a memory 130, a clock supply unit 140, and a reset control unit 150 all are integrated (Abstract; FIG. 1). The first processor 110 and second processor 120 operate synchronously with first and second internal clock signals ICLK1, ICLK2, respectively, which are generated by the clock supply unit 140 (FIG. 1; col. 3, lines 49-65). The reset control unit 150 supplies reset signals IRES1, IRES2, IRES3 to the clock supply unit 140, the first processor 110, and the second processor 120, respectively, in order to reset each of these system components (FIG. 1; col. 4, lines 6-13). The reset control unit 150 asserts IRES1, IRES2, and IRES3 based on the states of external reset signals, ERES1, ERES2, ERES3, which are input to reset control unit 150 (FIG. 1; col. 4, lines 18-20).

When one of the processors 110, 120 has completed its processing, the external reset signals are asserted to cause the reset control unit 150 to assert the corresponding internal reset signal, IRES2 or IRES3, which will cause the processor to reset (col. 5, lines 14-23). In addition, when one of the processors 110, 120 has completed its processing, clock supply unit 140 may terminate its internal clock signal (i.e., either ICLK1 or ICLK 2), thus reducing power dissipation (col. 6, lines 18-21).

Applicant's claims 1, 9, 10, 13, 17, and 22 (from which the remaining rejected claims depend) include at least the following features, which differentiate claims 1-4, 6-7, 9-15, 17, and 22 from that which is disclosed by Sririam, Tamura, Okabayashi or their combination (only claim 1 is excerpted below for brevity, as claims 9, 10, 13, 17, and 22 include similarly distinguishing features):

Claim 1:

". . . processing . . . the first digital samples in the first buffer and the second buffer for all known paths of the first group of symbols during a first symbol group duration, wherein the processor is clocked by a processor clock at a clock rate that is faster than and not synchronous with the sample rate;

disabling the processor upon completion of processing the first digital samples by gating off the processor clock, wherein the processor remains disabled through a remainder of the first symbol group duration;

simultaneously with processing the first digital samples, buffering second digital samples corresponding to a second group of symbols into the second buffer and a third buffer, . . . wherein the first symbol group duration represents a duration of time during which the second digital samples are buffered into the second buffer and the third buffer;

at a beginning of a second symbol group duration that occurs consecutively with an end of the first symbol group duration, enabling the processor to process the second digital samples . . ."

Neither Sririam, Tamura, Okabayashi nor their combination disclose each and every feature of claims 1-4, 6-7, 9-15, 17, and 22. Applicant has amended claims 1, 9, 10, 13, 17, and 22 to include one or both of the following features: a) buffering the digital samples from the receiver is capable of occurring while the processor is disabled; and b) enabling of the processor being triggered by completion of buffering the next set of digital samples to be processed and the occurrence of a beginning of a next symbol group. None of the references alone or in combination disclose these features, particularly in combination with the additional features of disabling the processor by gating off a processor clock upon completion of processing digital samples associated with a symbol group, and prior to an end of a symbol group duration.

The combination of references does not disclose the claimed features. Neither Sririam, Tamura, nor Okabayashi disclose methods or apparatus capable of receiving (from a receiver) and buffering a next set of digital samples to be processed by a processor *while the processor is disabled*. In addition, in Applicant's claims, the triggering event for disabling the processor is completion of processing digital samples, and the triggering events for re-

enabling the processor is the occurrence of the beginning of a symbol group duration and completion of buffering a next set of digital samples to be processed. Neither Sririam, Tamura, nor Okabayashi disclose any such triggering events.

Based on the above remarks, Applicant believes that the rejection of claims 1-4, 6-7, 9-15, 17, and 22 under 35 U.S.C. 103(a) has been overcome. Accordingly, Applicant respectfully requests that this rejection be reconsidered and withdrawn, and that claims 1-4, 6-7, 9-15, 17, and 22 be allowed.

Rejection of Claim 5:

Claim 5 is rejected under 35 U.S.C. §103(a) as being unpatentable over Sririam, Tamura, Okabayashi, and U.S. Patent No. 6,650,140 to Lee et al. (herein "Lee"). Applicant previously cancelled claim 5, and therefore this rejection is moot.

Rejection of Claim 16:

Claim 16 is rejected under 35 U.S.C. §103(a) as being unpatentable over Sririam, Tamura, and Okabayashi in view of U.S. Patent Publication No. 2002/0176489 to Roohparvar (herein "Roohparvar"). Applicant previously cancelled claim 16, and therefore this rejection is moot.

Rejection of Claims 18-21:

Claims 18-21 are rejected under 35 U.S.C. §103(a) as being unpatentable over Sririam in view of Tamura and Okabayashi, and further in view of U.S. Patent Publication No. 2001/0038633 to Robertson et al. Claims 18-21 are hereby cancelled, and therefore this rejection is now moot.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending are in condition for allowance. A Notice of Allowance is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (480) 385-5060. If necessary, the Commissioner is hereby authorized to charge payment or credit any overpayment to Deposit Account No. 50-2091 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly extension of time fees.

Respectfully submitted,

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